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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,606	02/26/2002	Michael Karl Gschwind	YOR920020001US1	8683

24299 7590 06/02/2005

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,606	GSCHWIND ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-18, and 20-27* is/are rejected.

7)☒ Claim(s) *6 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities:
    a. Line 2 contains a period in the middle of the claim. It appears that applicant intended to have the period instead be a comma.
    b. In line 6, please change the limitation "of reaching" to "to reaching".
2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-4, 9-12, 14-17, 22-25, and 27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Nemirovsky et al., US Patent Application Publication US 2002/0062435 (herein after Nemirovsky).
5. Referring to claim 1, Nemirovsky have taught in a processor, an apparatus for issuing instructions, wherein said processor has a memory (Figure 2, element 201). a decoding unit (Figure 2, element 203, page 4, paragraph [0040]), and an execution unit (Figure 2, elements 207, 208, 209, and 210, page 4, paragraphs [0042]-[0043]), said apparatus, comprising:

a. a classification logic adapted for prioritizing instructions in relation to one another and sorting said instructions in a number of priority categories (Figure 2, element 9, page 4), wherein said instructions come from said memory and are being decoded in said decoding unit prior of reaching said classification logic (Figure 2, page 4, paragraph [0040]);

b. a plurality of instruction queues, wherein said queues contain said instructions in decoded form (Figure 2, page 4, paragraph [0040]),wherein said plurality of said queues matches said number of said priority categories, and wherein each of said queues adapted to receive only one of said priority categories of said instructions from said classification logic, whereby said queues having same priority categories as said instructions (pages 4 and 5, paragraph [0040], Each stream has a respective queue where priority is assigned to each stream in static priority in descending order or where priority is assigned in a round robin fashion.); and

c. an issue logic to dispatch said instructions for execution in said execution unit of said processor, wherein said issue logic is operably coupled to said plurality of instruction queues and selecting from which of said queues to dispatch said instructions for execution, wherein said issue logic has been designed to be cognizant of said priority categories of said queues (Figure 2, elements 5 and 6, pages 3-5, paragraphs [0036]–[0061]).

6. Referring to claim 2, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus forms part of an in-order

instruction issue processor architecture (Page 4, The instructions are executed in the order of their priority.).

7. Referring to claim 3, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus forms part of an out-of-order instruction issue processor architecture (Page 4, paragraph [0043], reservation station).
8. Referring to claim 4, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said plurality of instruction queues consist of two queues, a high priority queue (pages 3-5, paragraphs [0036]–[0061], An instruction steam with the highest priority has a high priority queue.) and a low priority queue (pages 3-5, paragraphs [0036]–[0061], An instruction steam with the lowest priority has a low priority queue.).
9. Referring to claim 9, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said prioritizing of said instructions is based on a probability for memory miss (Page 6, paragraph [0066] - [0068]).
10. Referring to claim 10, Bain, Jr. et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus is designed for prioritizing and issuing said instructions in a static manner (abstract, page , paragraph [0044]).
11. Referring to claim 11, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus is designed for prioritizing and issuing said instructions in a dynamic manner (abstract).
12. Referring to claim 12, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus further comprising a predictor

unit operably coupled to said classification logic, wherein said predictor unit identifies performance-critical instructions (Page 5, paragraph [0059]).

13. Claim 14 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.
14. Claim 15 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.
15. Claim 16 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.
16. Claim 17 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.
17. Claim 22 does not recite limitations above the claimed invention set forth in claim 9 and is therefore rejected for the same reasons set forth in the rejection of claim 9 above.
18. Claim 23 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.
19. Claim 24 does not recite limitations above the claimed invention set forth in claim 11 and is therefore rejected for the same reasons set forth in the rejection of claim 11 above.
20. Claim 25 does not recite limitations above the claimed invention set forth in claim 12 and is therefore rejected for the same reasons set forth in the rejection of claim 12 above.
21. Referring to claim 27, Hum et al. have taught a program storage device, readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for issuing instructions as recited in claim 14 (Figure 2, pages 3-5, paragraphs [0036]–[0061]).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky et al., US Patent Application Publication US 2002/0062435 (herein after Nemirovsky), in view of Wulf et al., US Patent 6,154,826 (hereinafter Wulf).

24. Referring to claim 7, Nemirovsky has taught the apparatus for issuing instructions of claim 1, as described above. Nemirovsky has not taught wherein said prioritizing of said instructions is based on said instructions being scalar instructions or vector instructions. Wulf has taught wherein said prioritizing of said instructions is based on said instructions being scalar instructions or vector instructions (column 2, line 60-colum 3, line 37) for the desirable purpose of avoiding memory bottlenecks. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the prioritizing of the instructions in Nemirovsky based on said instructions being scalar instructions or vector instructions, as taught by Wulf, for the desirable purpose of avoiding memory bottlenecks (column 2, line 60-colum 3, line 37).

25. Claim 20 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

26. Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky et al., US Patent Application Publication US 2002/0062435 (herein after Nemirovsky), in view of Taniani et al., US Patent 5,655,114 (hereinafter Taniani).

27. Referring to claim 8, Nemirovsky has taught the apparatus for issuing instructions of claim 1, as described above. Nemirovsky has not specifically taught wherein said prioritizing of said instructions is based on a conditionality of branching. However, Taniani has taught prioritizing of said instructions is based on a conditionality of branching (column 3, lines 46-52, column 11, line 35-column 12, line 28) to minimize useless prefetch operations. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the prioritizing of Nemirovsky be based on a conditionality of branching, as taught by Taniani, for the desirable purpose of minimizing useless prefetch operations (column 3, lines 46-52, column 11, line 35-column 12, line 28).

28. Claim 21 does not recite limitations above the claimed invention set forth in claim 8 and is therefore rejected for the same reasons set forth in the rejection of claim 8 above.

29. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky et al., US Patent Application Publication US 2002/0062435 (herein after Nemirovsky), in view of Computer Architecture A Quantitative Approach, Hennessy and Patterson, pages 402 and 403 (hereinafter Hennessy).

30. Referring to claim 5, Nemirovsky has taught the apparatus for issuing instructions of claim 1, as described above. Nemirovsky has not specifically taught wherein said instructions sorted in said number of priority categories by said classification logic

comprise cloned instructions. However, Nemirovsky has recognized the need to prefetch instructions for execution (Page 4, paragraph [0040]). Hennssy has taught inserting prefetch, or cloned, instructions to improve the average memory access time significantly (Hennessy, pages 402 and 403). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the apparatus of Nemirovsky insert cloned prefetch instructions into the instruction stream, as taught by Hennessy, for the desirable purpose of improving the average memory access time significantly (Hennessy, pages 402 and 403). When the cloned prefech instructions are inserted into the instruction stream of Nemirovsky, it follows that the cloned perfetch instructions are sorted in said number of priority categories by said classification logic.

31. Claim 18 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

32. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky et al., US Patent Application Publication US 2002/0062435 (herein after Nemirovsky), in view of Panwar,US Patent 5,890,008 (hereinafter Panwar).

33. Referring to claim 13, Nemirovsky has taught the apparatus for issuing instructions of claim 1, as described above. Nemirovsky has not taught wherein said classification logic further adapted for receiving preannotated instructions, wherein said instructions have been preannotated during compilation time and said preannotations indicate said priority categories. However, Panwar has taught preannotating instructions during compile time to indicate a thread identification number for the desirable purpose of flushing only the instructions in a thread containing a mispredict (Figure 7, column 10, line 58-column 11,

line 7, column 13, lines 12-24). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the apparatus of Nemirovsky receive preannotated instructions, wherein said instructions have been preannotated during compilation time, as taught by Panwar, for the desirable purpose of flushing only the instructions in a thread containing a mispredict. Having the thread IDs, or preannotations of Panwar, in the instructions of Nemivorsky indicates the priory categories since each thread has a priority category. The thread ID is the priority category indication.

34. Claim 26 does not recite limitations above the claimed invention set forth in claim 13 and is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

Response to Arguments

35. Applicant's arguments with respect to claims 1-5, 7-18, and 20-27 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

36. Claim 6 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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